IN THE CLAIMS:

Please cancel claims 1-30 and add the following new claims. (All claims listed)

Claims 1-30 (Canceled)

31. (New) In a multi-threaded processor executing instructions for at least first and second threads, a method of assigning thread priority comprising:

determining whether instruction fetch operations for the first thread will be blocked due to processing of instructions for the second thread;

assigning priority to the first thread in said processor.

32. (New) The method of claim 31 further comprising;

setting a threshold counter to perform a counting operation in response to said determining operation.

33. (New) The method of claim 32 further comprising:

performing instruction fetch operations for the first thread after said threshold counter completes its counting operation.

34. (New) The method of claim 33 further comprising:

moving instructions in an execution pipeline of said processor from the second thread to a temporary storage area.

35. (New) In a processor to handle processing of at least first and second threads in parallel, a method of assigning thread priority comprising:

determining if a plurality of conditions for said first thread are true, the conditions including

if the processor is operating in a multithreaded processing mode;

if the first thread has no instructions in an execution pipeline of said processor; and

if the first thread is attempting to fetch instructions from a memory

determining that there is an indication of approaching instruction side starvation for said first thread if said plurality of conditions are true.

36. (New) The method of claim 35 further comprising:

setting a threshold counter to perform a counting operation if said plurality of conditions are true.

37. (New) The method of claim 36 further comprising:

resolving instruction starvation after said threshold counter completes its counting operation.

38. (New) The method of claim 35 further comprising:

resolving instruction starvation for said first thread by moving instructions in an execution pipeline of said processor from the second thread to a temporary storage area.

39. (New) A multi-threaded processor comprising:

first and second thread queues;

control logic coupled to said first and second thread queues, said control logic to determine whether instruction fetch operations for the first thread will be blocked due to processing of instructions for the second thread.

40. (New) The processor of claim 39 wherein said control logic is to assign priority to the first thread in said processor if instruction fetch operations for the first thread will be blocked due to processing of instructions for the second thread.

41. (New) The processor of claim 40, further comprising a threshold counter to perform a counting operation, wherein said control logic is to set said threshold counter if it is determined that instruction fetch operations for the first thread will be blocked due to processing of instructions for the second thread.

42. (New) The processor of claim 41 wherein said control logic assigns priority to said first thread after said threshold counter completes its counting operation.

43. (New) The processor of claim 42 further comprising an execution pipeline and a temporary storage area wherein said control logic is to move instructions in the execution pipeline of said processor from the second thread to the temporary storage area.